IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Andrew MacCormack et al.
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For	:	DIGITAL RECEIVER DEMULTIPLEXER
Examiner	:	Scott E. Beliveau
Art Unit	:	2623
Docket No.	:	858063.435
Date	:	December 8, 2006

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANTS' BRIEF

Commissioner for Patents:

This brief is in furtherance of the Notice of Appeal, filed in this case on June 8, 2006. The fees required under Section 41.20(b)(2), and any required request for extension of time for filing this brief and fees therefor, are dealt with in the accompanying transmittal letter.

I. REAL PARTY IN INTEREST

The real party in interest is STMicroelectronics Limited, which is the assignee of the present invention. The assignment of record is to STMicroelectronics Limited, having an address at 1000 Aztec West, Almondsbury, Bristol, BS32 4SQ United Kingdom.

II. RELATED APPEALS AND INTERFERENCES

Appellants, Appellants' legal representative, and the real party in interest are unaware of any appeal or interference which may be related to, directly affect, be directly affected by, or have a bearing on the Board's decision in the present appeal.

III. STATUS OF CLAIMS

Claims 1, 3-11, and 13-46 are currently pending in this application. All pending active claims are attached as Appendix A.

Claims 1, 3-11, 13-42, 45, and 46 stand rejected. Claims 1 and 3-10 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Claims 39-41, 45 and 46 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,959,659 issued to Dokic ("Dokic"). Claims 11 and 13-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dokic in view of the ADSP-2100 Family User's Manual – Chapter 4: Data Transfer (the "Manual"). Claims 21-38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dokic in view of U.S. Patent No. 5,844,595 issued to Blatter et al ("Blatter"). Claim 42 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dokic in view of U.S. Patent No. 5,602,920 issued to Bestler et al ("Bestler"). Id. Claims 43 and 44 have been indicated as having allowable subject matter, but these claims stand objected to as depending from a rejected base claim.

The rejections of claims 1, 3-11 and 13-46 are being appealed.

IV. STATUS OF AMENDMENTS

An Amendment under 37 C.F.R. § 1.116, filed after the Final Rejection, has not been entered by Examiner Beliveau (hereinafter "Examiner"). In the Amendment, Applicants sought to clarify the language of claims 1 and 3-10 to address the Examiner's concerns and to amend the drawings to address other concerns raised by the Examiner. The Amendment also contained new claims directed to the subject matter of allowable claims 43 and 44. Applicants subsequently offered to cancel the new claims, so that the issues in dispute could be clearly presented to the Board for review, but the Examiner indicated the Amendment would not be entered, even if the new claims were canceled. In the event of a remand, Applicants are prepared to resubmit the proposed amendments.

V. SUMMARY OF CLAIMED SUBJECT MATTER

This Application claims priority to Great Britain Application No. GB9802093, filed January 30, 1998. The following summary discusses the subject matter of the appealed claims along with references to portions of the specification and drawings that provide support

for the claims. The references are provided for exemplary purposes and are not intended to restrict the scope of the claims to the particular embodiments corresponding to the references provided.

The present invention generally relates to demultiplexing of a digital data stream in a receiver, so as to retain only those parts of the digital data stream required by the receiver. The invention relates particularly but not exclusively to such a receiver circuit in a television system having a digital set-top-box receiver.

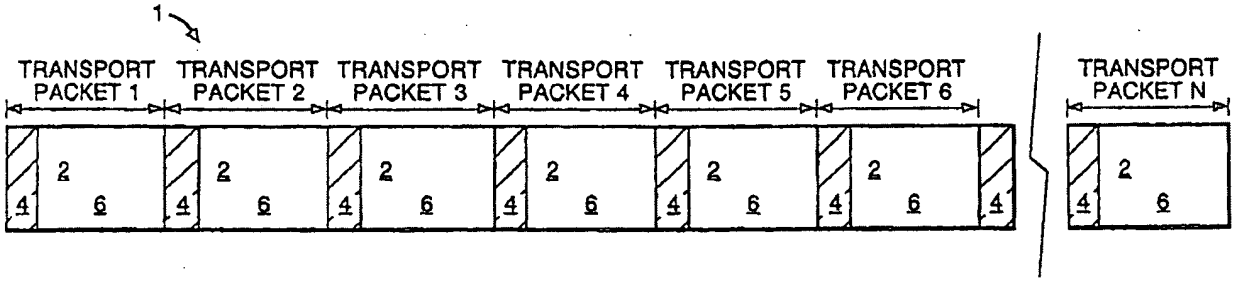

FIG. 1

Figure 1 of the present application, reproduced above for the Board's convenience, illustrates a portion of a transport stream 1 which is composed of a series of N transport packets 2. Each transport packet 2 comprises a transport packet header 4 and a transport packet payload 6. The transport stream is a bit stream which carries in the transport packet payloads 6 information for recreating, for example, a number of different television programs. The transport stream is formed by source encoding the television programs. The transport stream is then typically channel encoded for transmission (by satellite or cable) and channel decoded on its reception to reproduce the transport stream. The transport stream is then source decoded to recreate a selected one of the different television programs. A particular television program is recreated using three types of information (audio information, video information and tables of program information). Each transport packet 2 is preferably associated with a particular television program, a particular source encoding time and a particular one of the information types. The individual transport packets are time division multiplexed to form the transport stream and allow the real-time recreation of any one of the different television programs from the transport stream. To recreate a television program the transport stream is sequentially

demultiplexed to recover only the transport payloads 6 of audio information, video information and tables of program information which are associated with the selected television program. The recovered payloads are then decoded and used to recreate the television program.

An embodiment of the present invention provides a programmable transport interface in which the demultiplexing of an incoming data stream is programmable so as to enable different standards to be multiplexed without placing a burden on the main processor of the decoder.

An example embodiment of a programmable transport interface is illustrated in Figure 2, which is reproduced for the Board's convenience.

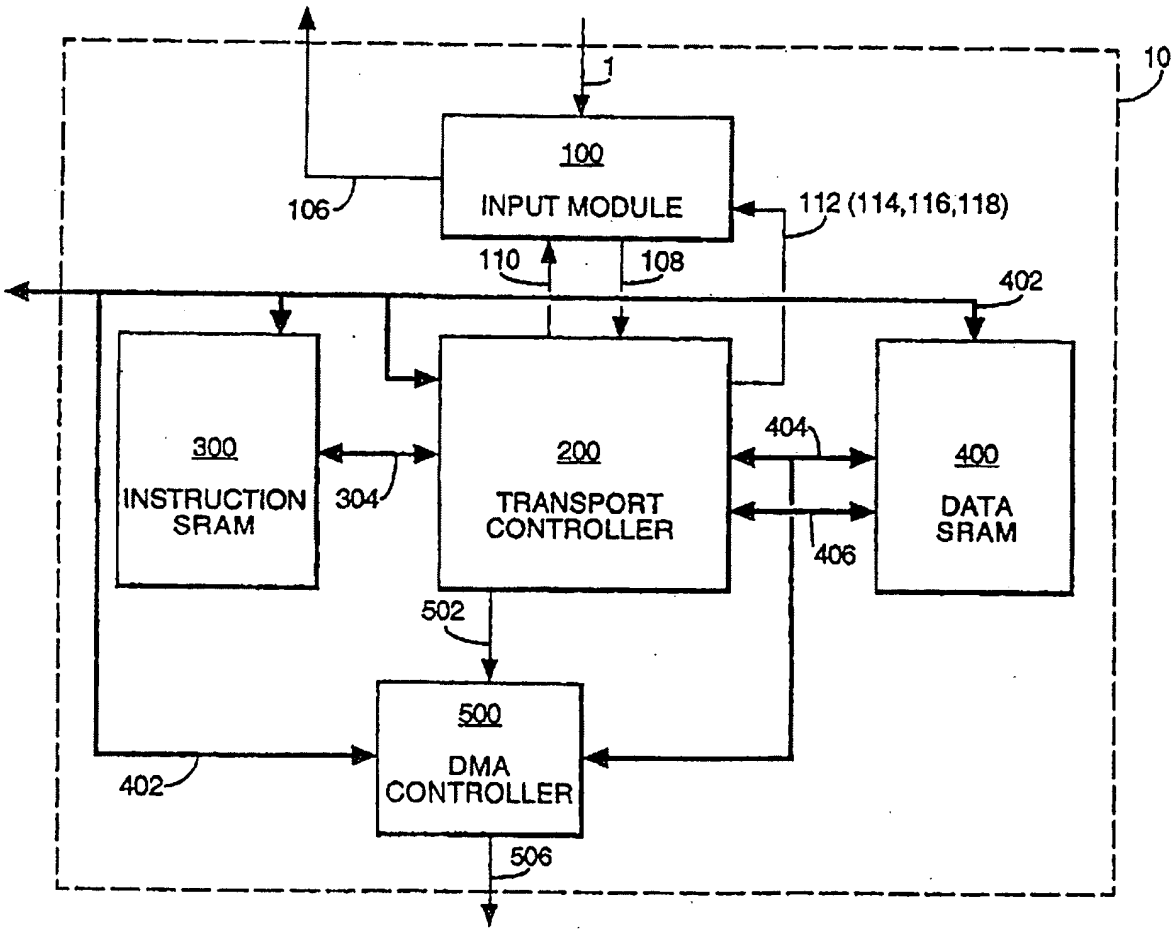

FIG. 2

For example, the embodiment of the receiver of **claim 1** demultiplexes a digital data stream, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver. The receiver comprises:

- an input module for receiving and processing the digital data stream;
- a memory for storing packet identifiers corresponding to data packets required by the receiver and separate from the input module;
- a first control circuit for controlling the storage in the memory of the packet identifiers;
- a second control circuit for extracting a packet identifier from a data packet in the digital data stream; and
- a third control circuit for receiving the extracted packet identifier and determining whether such matches one of the packet identifiers stored in the memory, for setting a match signal to the second control circuit responsive to a match, and for outputting an address in the memory responsive to a match, wherein the second control circuit accesses the address in the memory to retrieve control information associated with the packet identifier and controls processing of the input data packet responsive to the match signal by the input module.

Support for independent claim 1 can be found not only in Figure 2 but also in claim 1 as originally filed, on page 5, line 23, to page 6, line 5, Specification as Filed, and on page 4, line 28, to page 5, line 9, Substitute Specification. Additional support for claim 1 in the form of an example embodiment of a transport controller of the programmable transport interface is provided in Figure 3, reproduced below for the Board's convenience. Further support can be found in the description of Figure 3 provided on page 13, line 22, to page 16, line 18, Specification as Filed, and on page 11, line 27, to page 14, line 10, Substitute Specification.

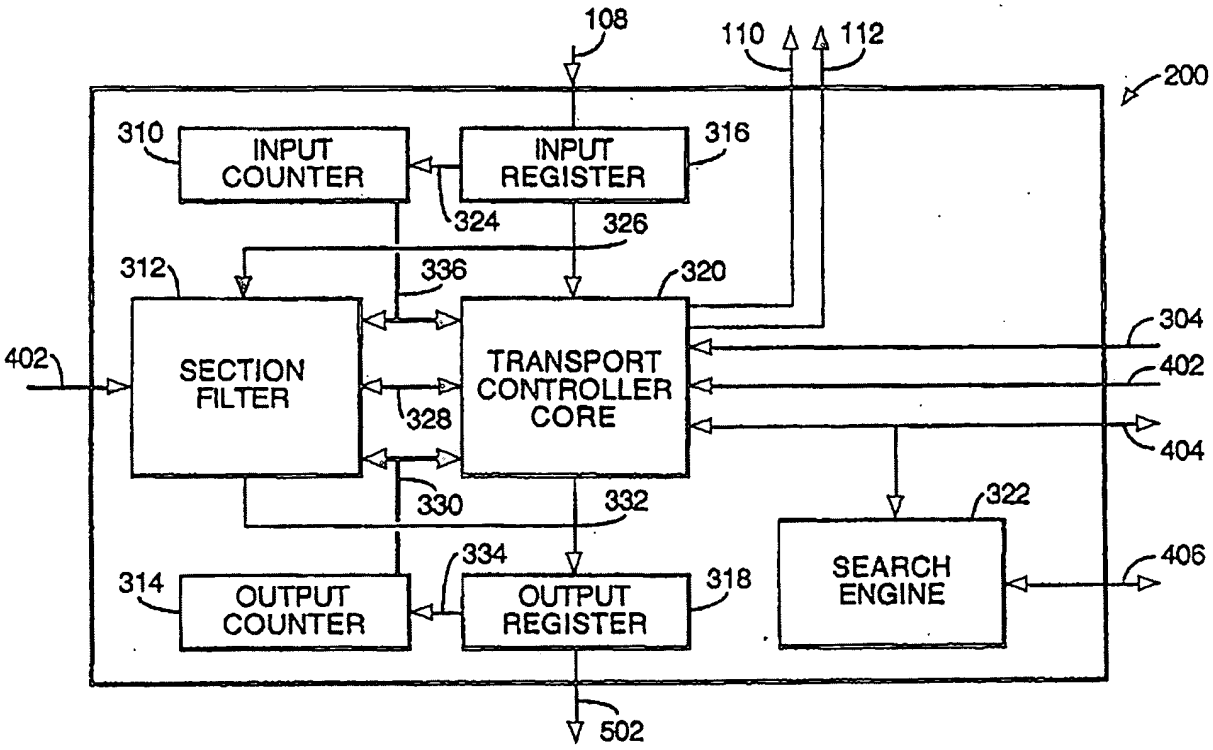

FIG. 3

In addition, support in the form of an example embodiment of the search engine of the transport controller of Figure 3 is provided in Figure 4, also reproduced below for the Board's convenience. Further support can be found in the description of Figure 4 provided on page 16, line 20 to page 23, line 22, Specification as Filed, and on page 14, line 11, to page 20, line 14, Substitute Specification.

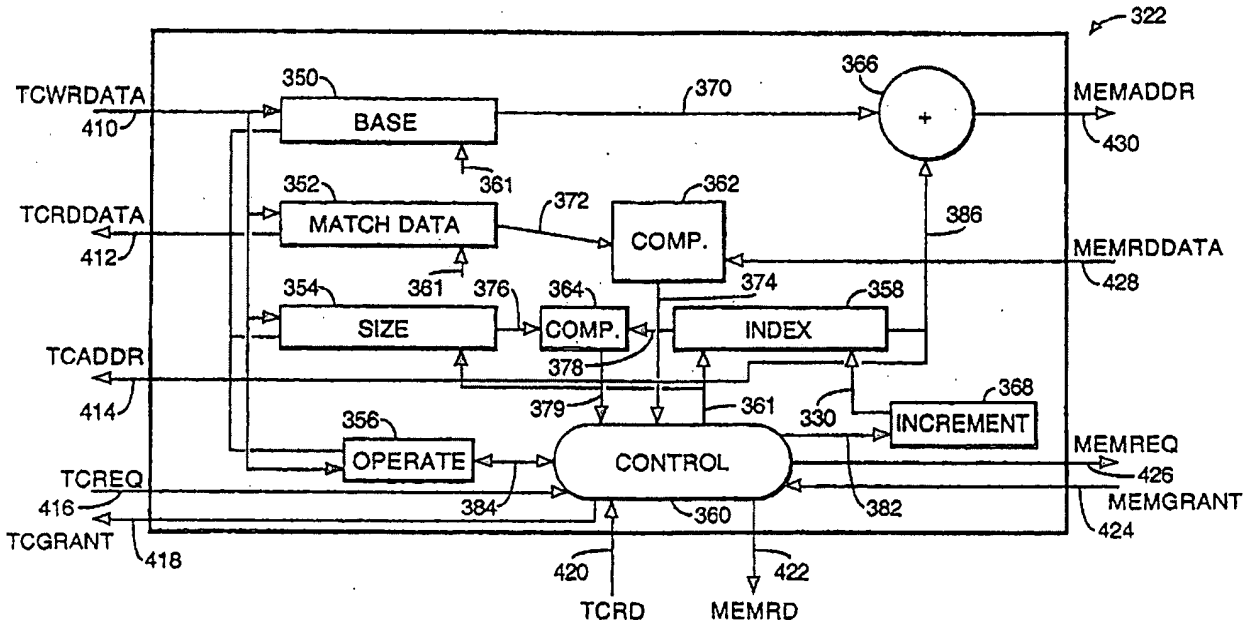

FIG. 4

An embodiment of the set top box of **claim 10** includes a receiver for demultiplexing a digital data stream, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, the receiver comprising the same elements as the receiver in claim 1. Support for the receiver as claimed in independent claim 10 can be found in the portions of the application listed above in reference to claim 1. Support for a set top box including a receiver can be found on page 1, lines 9-12, page 7, lines 10-13, Specification as Filed, and on page 1, lines 6-7, page 6, lines 10-12, Substitute Specification. Applicants submit that independent claims 1 and 10 do not contain any means-plus-function limitations.

An embodiment of a method of **claim 11** for demultiplexing a digital data stream input to a receiver, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, comprises the steps of:

- inputting the digital data stream;
- storing in a memory separate from the data stream and under the control of a first control circuit, packet identifiers of data packets required by the receiver;

- extracting, under the control of a second control circuit, a packet identifier from a data packet in the input digital data stream;
- determining, under the control of a third control circuit, whether the extracted packet identifier matches one of the stored packet identifiers;
- setting a match signal responsive to a match determined by the third control circuit;
- outputting, responsive to a match and under the control of the third control circuit, an address in the memory;
- accessing, under the control of the second control circuit, the address in memory;
- retrieving control information associated with the packet identifier and stored at such address; and
- demultiplexing, under the control of the second control circuit, the input data packet responsive to the match signal.

Support for independent claim 11 can be found in claim 11 as originally filed, on page 6, lines 3-17, Specification as Filed, and on page 5, lines 10-20, Substitute Specification. In another example, an embodiment of a method of **claim 20** for decoding a broadcast digital data signal in a set top box comprises steps substantially similar to those of claim 11. Support for the steps of independent claim 20 can be found in the portions of the application listed above in reference to claim 11. Support for decoding a broadcast digital data signal in a set top box can be found in claim 20 as originally filed, on page 1, lines 9-12, page 7, lines 10-13, Specification as Filed, and on page 1, lines 6-7, page 6, lines 10-12, Substitute Specification.

Applicants note that the Examiner objected to the Figures for failing to illustrate the steps recited in independent claims 11 and 20, and Applicants offered in their Response after Final to add a figure illustrating the recited steps (which were disclosed in the specification as filed). As noted above, the Amendment After Final was not entered. Applicants are prepared to amend the figures to address the Examiner's objection in the event of a remand. Applicants submit that independent claims 11 and 20 do not contain any step-plus-function limitations.

An embodiment of the receiver of **claim 21** includes a receiver for demultiplexing a digital data stream, the digital data stream including data packets each having a packet

identifier, so as to retain only those data packets required by the receiver, the receiver comprising:

- input circuitry for receiving the digital data stream;
- a first data structure for storing addressing information that is accessed based on packet identifiers;
- a second data structure for storing control information that is accessed based on addressing information extracted from the first data structure;
- a first control circuit for extracting a packet identifier from a data packet in the digital data stream input to the input circuitry; and
- a second control circuit for receiving the extracted packet identifier and determining whether such matches one of the packet identifiers in the first data structure, for setting a match signal to the first control circuit responsive to a match, and outputting addressing information responsive to a match, wherein the first control circuit accesses the second data structure to retrieve control information associated with the addressing information and demultiplexes the input data packet responsive to the match signal.

Support for independent claim 21 can be found in Figures 2 and 3. In addition, support in the form of an example embodiment of the advantageous interconnection of arrays, associated with transport packets, in the memory of the programmable transport interface of Figure 2 is provided in Figure 5, also reproduced below for the Board's convenience.

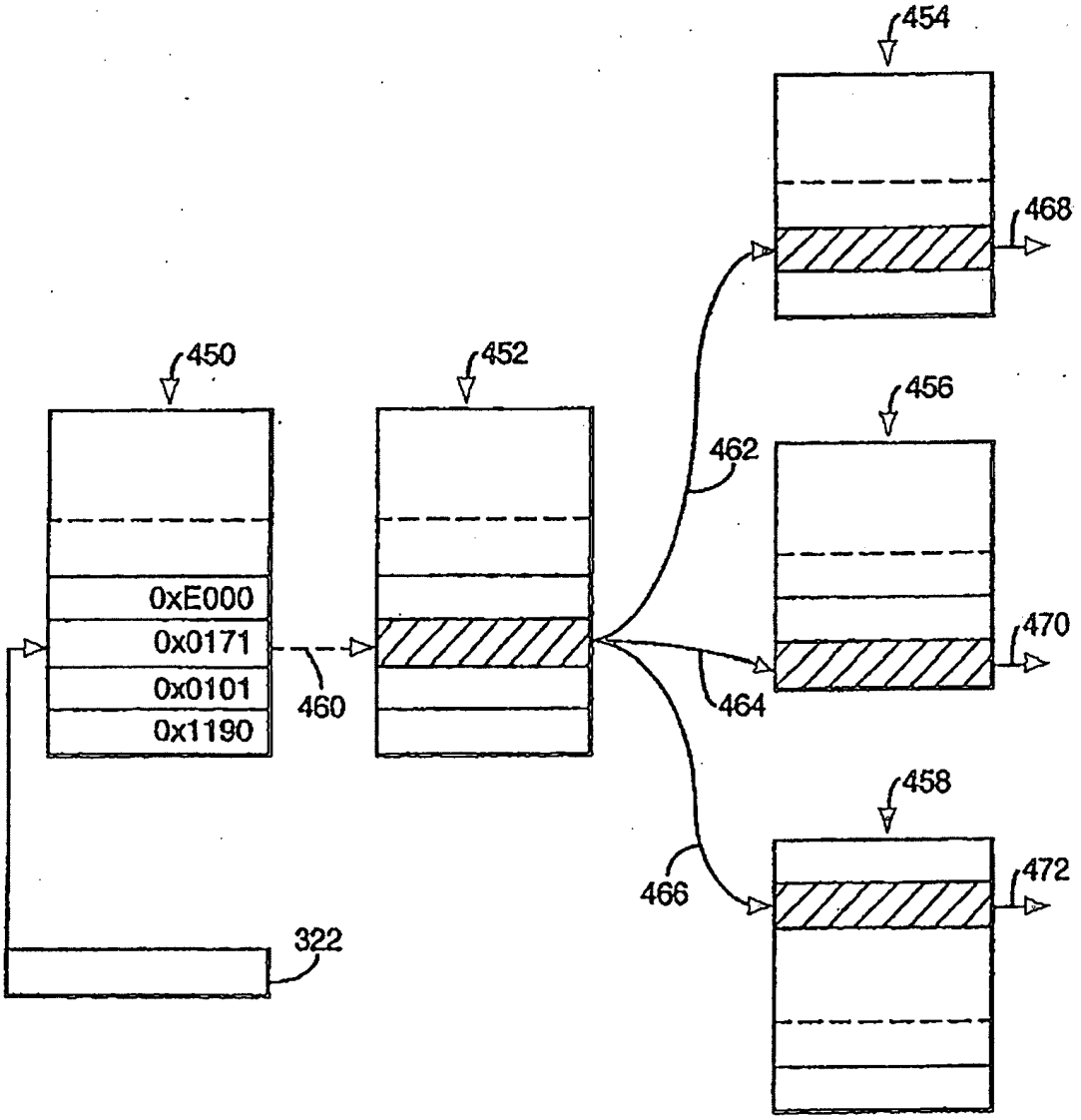

FIG. 5

Further support for claim 21 can be found in the description of Figure 5 provided on page 23, line 24 to page 24, line 11, Specification as Filed, and on page 20, line 15, to page 21, line 3, Substitute Specification. An embodiment of the set top box of **claim 29** includes a receiver for demultiplexing a digital data stream, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, the receiver comprising the same elements as the receiver of claim 21. Support for the receiver

as claimed in independent claim 29 can be found in the portions of the application listed above in reference to claim 21. Support for a set top box including a receiver can be found on page 1, lines 9-12, page 7, lines 10-13, Specification as Filed, and on page 1, lines 6-7, page 6, lines 10-12, Substitute Specification.

More detail in the form of an example embodiment of a digital broadcast system incorporating a programmable transport interface is provided in Figure 6, also reproduced below for the Board's convenience. Further support can be found in the description of Figure 6 provided on page 24, line 13 to page 27, line 5, Specification as Filed, and on page 21, line 4, to page 23, line 15, Substitute Specification.

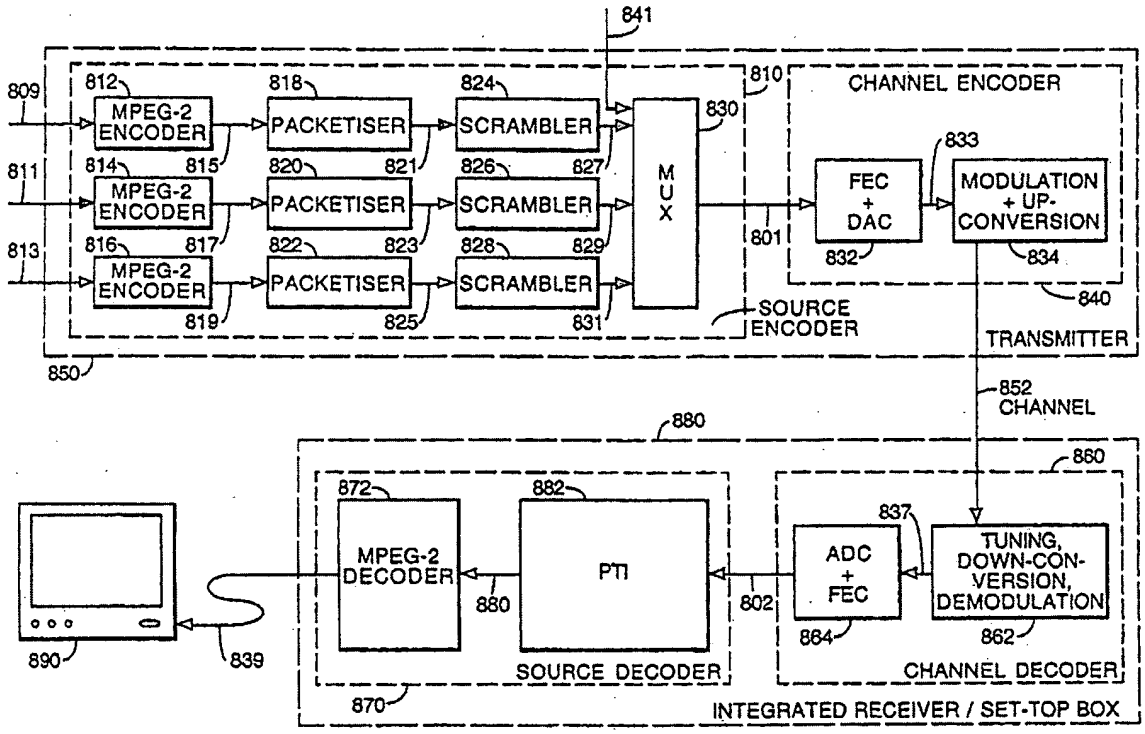

FIG. 6

Applicants submit that independent claims 21 and 29 do not contain any means-plus-function limitations.

An embodiment of a method of demultiplexing a digital data stream of **claim 30,** the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, comprises the steps of:

inputting the digital data stream;

storing control information in a first data structure;

storing packet identifiers and corresponding addressing information in a second data structure;

extracting, under the control of a first control circuit, a packet identifier from a data packet in the input digital data stream;

determining, under the control of a second control circuit, whether the extracted packet identifier matches one of the packet identifiers in the second data structure;

setting a match signal responsive to a match determined by the second control circuit;

outputting addressing information from the second data structure responsive to a match;

retrieving, under control of the first control circuit and based on the outputted addressing information, control information from the first data structure; and

demultiplexing, under the control of the first control circuit, the input data packet responsive to the match signal.

Support for independent claim 30 can be found can be found in Figure 5, the description of Figure 5 provided on page 23, line 24 to page 24, line 11, Specification as Filed, and on page 20, line 15, to page 21, line 3, Substitute Specification. An embodiment of the method of decoding a broadcast digital data signal in a set top box of **claim 38** includes the same steps as the method of claim 30. Support for the method as claimed in independent claim 38 can be found in the portions of the application listed above in reference to claim 30. Support for a set top box including a receiver can be found on page 1, lines 9-12, page 7, lines 10-13, Specification as Filed, and on page 1, lines 6-7, page 6, lines 10-12, Substitute Specification.

More detail in the form of an example embodiment of a digital broadcast system incorporating a programmable transport interface is provided in Figure 6, also reproduced above for the Board's convenience. Further support can be found in the description of Figure 6 provided on page 24, line 13 to page 27, line 5, Specification as Filed, and on page 21, line 4, to page 23, line 15, Substitute Specification.

Applicants submit that independent claims 30 and 38 do not contain any step-plus-function limitations.

In another example, an embodiment of the receiver of **claim 39** for processing a packetized digital data stream includes:

- an input module to receive and process a data packet;
- a memory;
- a receiver processor to control storage of desired packet identifiers and associated control information in the memory; and
- a transport controller having a transport processor to extract a packet identifier from a packet in the input module and a search engine to search the memory for a match of the extracted packet identifier to a desired packet identifier stored in the memory, wherein responsive to a match the transport processor retrieves from the memory control information associated with the desired packet identifier stored in the memory and controls processing of the received data packet by the input module based on the retrieved control information.

Support for independent claim 39 can be found not only in Figure 2 but also in the description of Figure 2 found on page 8, line 17, to page 13, line 20, Specification as Filed (filed on January 29, 1999), and on page 7, line 12, to page 11, line 26, Substitute Specification (filed on November 14, 2002).

The embodiment of claim 42 additionally includes the transport processor generating a control signal to control processing of a packet by the input module based on associated control information retrieved from the memory and "wherein the input module descrambles a packet in response to the control signal." Support for the embodiment of claim 42 can be found in Figure 2 and the description of Figure 2 found on page 8, line 17, to page 13, line 20, Specification as Filed, and on page 7, line 12, to page 11, line 26, Substitute Specification.

As another example, the embodiment of claim 43 additionally includes the transport processor generating a control signal to control processing of a packet by the input module based on associated control information retrieved from the memory and "wherein the input module passes a data payload to the transport controller in response to the control signal."

Support for the embodiment of claim 43 can be found in Figure 2 and the description of Figure 2 found on page 8, line 17, to page 13, line 20, Specification as Filed, and on page 7, line 12, to page 11, line 26, Substitute Specification.

The embodiment of claim 44 additionally includes the transport processor generating a control signal to control processing of a packet by the input module based on associated control information retrieved from the memory, the input module passing a data payload to the transport controller in response to the control signal, and "wherein the transport controller reformats the data payload based on the control information and passes the reformatted data payload to the input module for output in an alternative output stream." Support for the embodiment of claim 44 can be found in Figure 2 and the description of Figure 2 found on page 8, line 17, to page 13, line 20, Specification as Filed, and on page 7, line 12, to page 11, line 26, Substitute Specification.

Independent **Claim 45** and **Claim 46** include means plus function elements. According to 37 C.F.R. § 41.37(c)(1)(v), such means plus function elements "must be identified and the structure, material, or acts described in the specification as corresponding to each claimed function must be set forth with reference to the specification by page and line number, and to the drawing, if any, by reference characters." Accordingly, the following shows claims 45 and 46 together with the required information in parentheses.

45. A receiver for processing a packetized digital data stream, the receiver comprising:

means for receiving a data packet in the digital data stream **(page 8, lines 17-22; page 8, line 35, to page 9, line 12; page 9, lines 22-26; page 26, lines 31-32; Specification as Filed) (page 7, lines 12-16; page 7, line 24, to page 8, line 6; page 8, lines 12-15; page 23, lines 7-8; Substitute Specification);**

means for retrieving control information associated with a received data packet **(page 11, lines 18-35; page 15, lines 24-33; page 16, lines 10-18; page 18, lines 11-17; page 21, lines 19-24; page 23, lines 4-13; page 26, lines 34-36; Specification as Filed) (page 10, lines 3-15; page 13, lines 19-25; page 14, lines 5-10; page 15, line 27, to page 16, line 2; page 18, lines 21-25; page 20, lines 3-9; page 23, lines 9-11; Substitute Specification);** and

means for controlling processing of a received data packet by the means for receiving a data packet **(page 9, line 28, to page 10, line 13; page 10, lines 25-28; page 11, lines 35-37; page 12, lines 9-11; page 22, lines 8-13; page 26, lines 31-32; page 26, lines 34-36; Specification as Filed) (page 8, line 16, to page 9, line 3; page 9, lines 11-13; page 10, lines 15-16; page 10, lines 22-24; page 19, lines 10-13; page 23, lines 7-8; page 23, lines 9-13; Substitute Specification)**.

46. The receiver of claim 45 wherein the means for retrieving control information comprises a memory storing packet identifiers and control information associated with desired data packets in the digital data stream, a search engine and a transport processor **(page 15, lines 24-33; page 16, lines 10-18; Specification as Filed) (page 13, lines 19-25; page 14, lines 5-10; Substitute Specification)**.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 1 and 3-10 comply with the written description and enablement requirements of 35 U.S.C. § 112, first paragraph.

2. Whether claims 39-41 are anticipated under 35 U.S.C. § 102(e) by Dokic.

3. Whether claims 45 and 46 are anticipated under 35 U.S.C. § 102(e) by Dokic.

4. Whether claims 11 and 13-20 are rendered obvious under 35 U.S.C. § 103(a) by Dokic in view of the Manual.

5. Whether claims 21-38 are rendered obvious under 35 U.S.C. § 103(a) by Dokic in view of Blatter.

6. Whether claim 42 is rendered obvious under 35 U.S.C. § 103(a) by Dokic in view of Bestler.

7. Whether claims 43 and 44, which the Examiner has indicated as having allowable subject matter, depend from a properly rejected base claim.

VII. ARGUMENT

Although the Examiner has rejected each of claims 1, 3-11, 13-42, 45, and 46 under either 35 U.S.C. §§ 102, 103, or 112, Final Office Action, the Examiner has not made out a *prima facie* case on any of the grounds for rejection.

A. Claims 1 and 3-100 Are Enabled and Comply With the Written Description Requirement

To support the written description and enablement rejections, the Examiner bears the initial burden of establishing that the written description in the specification is inadequate to enable any person skilled in the art to make and use the invention. To establish a *prima facie* case of lack of enablement, the Examiner "bears the burden of setting forth a reasonable explanation as to why it believes that the scope of protection by that claim is not adequately enabled by the description of the invention provided in the specification of the application; this includes, of course, providing sufficient reasons for doubting any assertions in the specification as to the scope of enablement." *In re Wright*, 999 F.2d 1557, 1561-1562 (Fed. Cir. 1993). Regarding written description, the Examiner must establish that the disclosure of the application does not reasonably convey to a person of ordinary skill in the art that the inventor had possession of the invention when the application was filed. Vas-Cath, Inc. v. Mahurkar, 935 F.2d 1555, 1563-1564 (Fed. Cir. 1991).

In the Final Office Action, the Examiner rejected Claims 1 and 3-10 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement and as not enabled. The Examiner's argument is based on a misinterpretation of the claims. Specifically, the Examiner contends the claim 1 and 10 recite an input module setting a match signal. Claims 1 and 10, however, do not recite an input module setting a match signal.

Claim 1 recites a receiver for demultiplexing a digital data stream, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, the receiver comprising an input module for receiving and processing the digital data stream; a memory for storing packet identifiers corresponding to data packets required by the receiver and separate from the input module; a first control circuit for controlling the storage in the memory of the packet identifiers; a second control circuit for extracting a packet identifier from a data packet in the digital data stream; and a ***third control***

circuit for receiving the extracted packet identifier and determining whether such matches one of the packet identifiers stored in the memory, ***for setting a match signal*** to the second control circuit responsive to a match, and for outputting an address in the memory responsive to a match, wherein the second control circuit accesses the address in the memory to retrieve control information associated with the packet identifier and controls processing of the input data packet responsive to the match signal by the input module. Appendix A, Claim 1 (emphasis added).

As also amended, claim 10 recites a set top box including a receiver for demultiplexing a digital data stream, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver. Appendix A, Claim 10. The receiver of claim 10 comprises the same elements as the receiver in claim 1 above. *Id.*

The Examiner notes that the specification discloses that the match signal is generated by the third control circuit. Final Office Action, Page 7. Applicants agree that some embodiments described in the specification (as well as those claimed in claims 3 and 10) involve the third control circuit generating a match signal under certain circumstances. See Figures 1-3, claim 1 as originally filed, the Specification as filed on page 5, line 23, to page 6, line 5, page 13, line 22, to page 16, line 18. The Examiner then argues that both claim 1 and claim 10 specify that the input module sets the match signal, and therefore rejects both claims as failing to comply with the written description requirement. Id. However, claims 1 and 10 do not specify that the input module sets the match signal. See Claims 1 and 10 ("a ***third control circuit*** ... ***for setting a match signal*** to the second control circuit responsive to a match") (emphasis added). The Examiner's rejection is based on a misreading of both claims. The Examiner's own analysis on page 7 of the Final Office Action states "the particular match signal as disclosed in the specification and **required by the claim to be generated by the 'third control circuit.'**[*sic*]" (emphasis added). Thus, there is no confusion about whether the input module or the third control circuit sets the match signal, and the claims do not recite the input module generating the match signal.

Claims 3-9 depend from claim 1. Appendix A. For the foregoing reasons, the Examiner has not established a prima facie case of non-enablement or lack of written description, and thus, the Section 112 rejections of claims 1 and 3-10 should be withdrawn.

B. *Claims 39-41 Are Not Anticipated by Dokic*

Under 35 U.S.C. § 102, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Here, the Examiner has failed to establish a *prima facie* case of anticipation for claims 39-41, 45, or 46. The Examiner erred in asserting that Dokic teaches or enables each of the claimed elements, either expressly or inherently, as interpreted by one of ordinary skill in the art.

Independent claim 39 recites: "A receiver for processing a packetized digital data stream, the receiver comprising: an input module to receive and process a data packet; a memory; a receiver processor to control storage of desired packet identifiers and associated control information in the memory; and a transport controller having a transport processor to extract a packet identifier from a packet in the input module and a search engine to search the memory for a match of the extracted packet identifier to a desired packet identifier stored in the memory, wherein responsive to a match the transport processor retrieves from the memory control information associated with the desired packet identifier stored in the memory and controls processing of the received data packet by the input module based on the retrieved control information." Claims 40 and 41 depend from claim 39.

The Examiner points to demultiplexer section 104 as the claimed input module, memory 205 as the claimed memory, host processor 106 as the claimed receiver processor, and digital signal processor 102 as the claimed transport processor, and to the description thereof at column 7, l. 49, through col. 9, l. 6, and col 13, ln. 13-26.

There is no indication in the cited portion of Dokic that the host processor 106 controls storage of desired packet identifiers ***and*** associated control information in the memory 205. The cited portion of Dokic refers to loading a PID filtering table from the host processor 106 into the memory 205. Dokic then defines the PID filtering table as containing the desired PIDs. There is no suggestion that the PID filtering table contain associated control information, or that such information be stored anywhere else in the memory 205. *See* Dokic, column 8, ln.

26-53. In addition, there is no indication in the cited portion of Dokic that the digital signal processor 102, responsive to a match, retrieves from the memory 205 control information associated with the desired packet identifier. Accordingly, Dokic does not anticipate claims 39-41.

To the extent the Examiner suggests that the type of packet is the "associated control information," Dokic does not teach, suggest or motivate storing the type of packet in the memory 205 (or retrieving the type of packet from the memory 205). Instead, Dokic teaches that the location in the PID filtering table where the PID is stored corresponds to the type of data packet. To the extent the Examiner points to the discussion of selecting a default program in Dokic (see col. 8, ln. 53-67), the default program data in Dokic is recovered from the transport stream when a PID filtering table is not available from the host processor 106. There is no suggestion in Dokic that the host processor 106 controls the storage of default PIDs in the memory 205 (or the storage of associated control information in the memory 205).

C. Claims 45 and 46 Are Not Anticipated by Dokic

Independent claim 45 separately recites: "means for receiving a data packet in the digital data stream; means for retrieving control information associated with a received data packet; and means for controlling processing of a received data packet by the means for receiving a data packet." As discussed above, Dokic does not teach, motivate or suggest retrieving control information associated with a received data packet. Claim 46 depends from claim 45 and further specifies that the means for retrieving control information comprises "a memory storing packet identifiers and control information associated with desired data packets in the digital data stream, a search engine and a transport processor." Accordingly, Applicants respectfully submit that claims 39-41, 45 and 46 are not anticipated by Dokic.

D. The Examiner has Failed to Establish a Prima Facie *Case that Dokic in view of the Manual Renders Claims 11 and 13-20 Obvious.*

The Examiner initially bears the burden of establishing a *prima facie* case of obviousness. In re Bell, 26 U.S.P.Q.2d 1529 (Fed. Cir. 1993); In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984); MPEP § 2142. An Applicant may

attack an obviousness rejection by showing that the Examiner has failed to properly establish a *prima facie* case or by presenting evidence tending to support a conclusion of non-obviousness. In re Fritch, 972 F.2d at 1265.

In order for an examiner to establish a *prima facie* case that an invention, as defined by a claim at issue, is obvious the examiner must: (1) show some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine the reference teachings; (2) there must be a reasonable expectation of success; and (3) the prior art reference (or the combined references) must teach or suggest all the claim limitations. MPEP § 2142. "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure." MPEP § 2143. The level of skill in the art cannot be relied upon to provide the suggestion to combine the references. MPEP § 2143.01 (citing Al-Site Corp. v. VSI Int'l Inc., 174 F.3d 1308, 50 U.S.P.Q.2d 1161 (Fed. Cir. 1999)). The mere fact that the references ***can*** be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. MPEP § 2143.01 (citing In re Mills, 916 F.2d 680, 16 U.S.P.Q. 2d 1430 (Fed. Cir. 1990)).

Moreover, a reference must be viewed as a whole, including portions that would lead away from the claimed invention. MPEP § 2141.03 (citing W.L. Gore & Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 220 U.S.P.Q. 303 (Fed. Cir. 1983)). If the proposed modification would change the principles of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. MPEP § 2143.01 (citing In re Ratti, 270 F.2d 810, 123 U.S.P.Q. 349 (CCPA 1959)).

Here, the Examiner has failed to establish a *prima facie* case of obviousness for claims 11, 13-20. The Examiner has rejected Claims 11 and 13-20 under 35 USC 103(a) as rendered obvious over Dokic in view of the ADSP-2100 Family User's Manual – Chapter 4: Data Transfer. Applicants respectfully traverse the Examiner's rejection.

Independent claims 11 and 20 recite, "inputting the digital data stream; storing in a memory separate from the data stream and under the control of a first control circuit, packet identifiers of data packets required by the receiver; extracting, under the control of a second control circuit, a packet identifier from a data packet in the input digital data stream;

determining, under the control of a third control circuit, whether the extracted packet identifier matches one of the stored packet identifiers; setting a match signal responsive to a match determined by the third control circuit; outputting, responsive to a match and under the control of the third control circuit, an address in the memory; accessing, under the control of the second control circuit, the address in memory; retrieving control information associated with the packet identifier and stored at such address; and demultiplexing, under the control of the second control circuit, the input data packet responsive to the match signal," (or similar language).

Dokic is not an appropriate primary reference because the Examiner is using an unreasonable interpretation of the claimed memory to include the memory 205 **and** data buffers 200 and 202 of Dokic. Buffers 200 and 202 are not separate from the data stream and do not store "packet identifiers corresponding to data packets required by the receiver" for determining "whether the extracted packet identifier matches one of the stored packet identifiers." Buffers 200 and 202 are circular buffers controlled by framing logic to load **all** data packets in the transport stream, whether the packets are required or not. See Column 7, line 66 to Column 8, line 19. Thus, buffers 200 and 202 are not separate from the data stream. Thus, Dokic is not an appropriate primary reference for claims 11 and 13-20.

The Examiner first argues that the buffers 200 and 202 meet the claim limitations for the memory if they store desired packet identifiers even for an instant. The Examiner ignores the limitation that the memory storing the packet identifiers be "separate from the data stream." The Examiner next argues that the specification discloses buffers in the data stream and storage of data packets from the data stream in the memory. The Examiner fails to provide specific citations to the specification and does not tie this argument to corresponding limitations in the claims. In any event, the specification as originally filed separately illustrates and describes the data stream. *See, e.g.* Original Specification, Figures 1 and 2 and the description thereof on pages 7-12. An embodiment of the data stream is illustrated and described as comprising the transport stream 1, the input module 100, interconnect 108, interconnect 110, the alternative output stream 106, the transport controller 200, the interconnect 502, the direct memory access controller 500 and the data output stream 506. See Figures 2 and 3. The specification as originally filed also separately illustrates and describes the data SRAM 400. *See, e.g.*, Figure 2 and the description of the data SRAM 400 on pages 11-13. There is no suggestion that the data

stream or the transport stream includes the data SRAM 400, passes through the data SRAM 400, or is buffered in the data SRAM 400, and Applicants respectfully submit one of skill in the art would not interpret the specification in this manner. Applicants further note that the claims do not address whether the transport stream comprises input buffers, or prohibit the memory from also storing data packets (or portions thereof).

Further, the Examiner admits that Dokic does not disclose or suggest "outputting an address", but claims this is suggested by the Manual, which describes the operation of a circular buffer. The problem with this argument is that the circular buffer of Dokic that the Examiner suggests combining with the Manual is the circular buffer 200/202, which the Examiner admits stores the "entire packet" and which as discussed above cannot be the claimed memory as recited. Accordingly, Applicants respectfully submit claims 11 and 13-20 are not rendered obvious by Dokic taken in combination with the Manual. Furthermore, if Dokic were modified such that the circular buffers stored either packet identifiers required by the receiver or addressing information, Dokic would not function as intended, as the stored information would be replaced (and thus lost) if the buffers were operated in a circular fashion and there would be no place to store the digital data stream as it was received if the buffers were not operated in a circular fashion or were used to store other information. Further, to the extent the address is an address of one of the buffers, it is still an address of a buffer in the data stream, and thus would not be an address in a memory separate from the data stream, as recited. Accordingly, Applicants respectfully submit that claims 11 and 13-20 are not rendered obvious by the combination of Dokic and the Manual.

E. The Examiner has Failed to Establish a Prima Facie *Case that Dokic in View of Blatter Renders Claims 21-38 Obvious.*

Claims 21-38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dokic in view of Blatter. Applicants respectfully traverse the Examiner's contention that claims 21-38 are obvious over Dokic in view of Blatter and further submit that the Examiner has failed to establish a *prima facie* case of obviousness. The Examiner's burden of proof is set forth above.

Claims 21 and 29 recite "a first data structure for storing addressing information that is accessed based on packet identifiers ... a second data structure for storing control

information that is accessed based on addressing information extracted from the first data structure ... outputting addressing information responsive to a match ... wherein the first control circuit accesses the second data structure to retrieve control information associated with the addressing information." Similarly, claim 30 recites ""storing control information in a first data structure; storing packet identifiers and corresponding addressing information in a second data structure ... outputting addressing information from the second data structure responsive to a match [and] retrieving ... based on the outputted addressing information, control information from the first data structure" and claim 38 similarly recites "storing, in a first data structure, control information; storing, in a second data structure, packet identifiers ... and addressing information corresponding to the packet identifiers ... outputting, responsive to a match, addressing information stored in the second data structure [and] retrieving ... based on the outputted addressing information, control information from the first data structure."

The Examiner admits that Dokic does not disclose or suggest the claimed first **and** second data structures. The Examiner contends memory 205 of Dokic is a first data structure, without explaining how or whether it satisfies the claim limitations. The Examiner also points to units 45 of Blatter as both the first data structure and the second data structure. The Examiner does not identify how to combine unit 45 with Dokic so as to achieve the claimed invention. Further, one of skill in the art would not be motivated to combine Dokic with Blatter. Dokic is directed to "a decoder having a decoupled hardware architecture for demultiplexing and decoding a digital data stream." Dokic, Column 1, lines 6-9. Dokic specifically decouples demultiplexing from decoding the digital data stream and expressly limits the "interpretation capabilities" of the digital signal processor 102 in order to speed up the demultiplexing so data can promptly be displayed. Dokic, Column 4, lines 48-60. The only data Dokic indicates is stored in the memory 205 is the PID look-up table, which Dokic teaches preferable contains only the required PIDs. There is no teaching or suggestion in Dokic that the PID look-up table contain addressing information that is accessed based on packet identifiers or control information that is accessed based on addressing information. Modifying the digital signal processor 102 of Dokic to contain two data structures with the second data structure containing control information to be retrieved and either employed by the digital signal processor to interpret the data stream or provided to an external circuit by the digital signal processor would defeat the

purpose of limiting the capabilities of the digital signal processor in order to speed up the demultiplexing, and would change the principles of operation of Dokic. *See* MPEP § 2143.01(VI) ("The proposed modification cannot change the principle of operation of a reference."); *In re Ratti*, 270 F.2d 810, 813, 123 U.S.P.Q. 349, 352 (C.C.P.A. 1959). Claims 22-28 depend from claim 21 and claims 31-37 depend from claim 30. Accordingly, Applicants submit that claims 21-38 are not rendered obvious by Dokic in view of Blatter, and the Examiner has failed to establish a *prima facie* case of obviousness.

F. *The Examiner has Failed to Establish a* Prima Facie *Case that Dokic in View of Bestler Renders Claim 42 Obvious.*

Claim 42 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dokic in view of Bestler. Applicants respectfully traverse the Examiner's contention that claim 42 is obvious over Dokic in view of Bestler. The Examiner's burden of establishing a *prima facie* case is set forth above.

Claim 42 depends from claim 39. The Examiner does not contend that the features of claim 39 that are missing from Dokic, as discussed above, are taught, suggested or motivated by Bestler.

Accordingly, Applicants respectfully submit that claim 42 is not rendered obvious by Dokic in view of Bestler and that the Examiner has not established a *prima facie* case of obviousness.

G. *The Allowable Subject Matter of Claims 43-44 Do Not Depend From a Validly Rejected Base Claim.*

Claims 43 and 44 have been indicated as having allowable subject matter, but these claims stand objected to as depending from a rejected base claim. As noted above, Applicants respectfully traverse the Examiner's contention that claim 39, from which claims 43 and 44 ultimately depend, is a validly rejected base claim. Accordingly, Applicants traverse the objections to claims 43 and 44 as well.

VIII. CLAIMS APPENDIX

A copy of the claims involved in the appeal are attached hereto as Appendix A.

IX. EVIDENCE APPENDIX

The Final Office Action referred to above is attached as Appendix B.

X. RELATED PROCEEDINGS APPENDIX

The Related Proceedings Appendix is attached as Appendix C. Applicants note that there are no related proceedings of which Applicants are aware.

Respectfully submitted,
Seed Intellectual Property Law Group PLLC

/Timothy L. Boller/

Timothy L. Boller
Registration No. 47,435

TLB:rr
Enclosures:
Appendix A
Appendix B
Appendix C

701 Fifth Avenue, Suite 5400
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031

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APPENDIX A

Claims Involved in the Appeal

1. A receiver for demultiplexing a digital data stream, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, the receiver comprising:

an input module for receiving and processing the digital data stream;

a memory for storing packet identifiers corresponding to data packets required by the receiver and separate from the input module;

a first control circuit for controlling the storage in the memory of the packet identifiers;

a second control circuit for extracting a packet identifier from a data packet in the digital data stream; and

a third control circuit for receiving the extracted packet identifier and determining whether such matches one of the packet identifiers stored in the memory, for setting a match signal to the second control circuit responsive to a match, and for outputting an address in the memory responsive to a match, wherein the second control circuit accesses the address in the memory to retrieve control information associated with the packet identifier and controls processing of the input data packet responsive to the match signal by the input module.

3. The receiver of claim 1 wherein responsive to the control information the second control circuit controls the transfer of the input data packet to a destination address identified by the control information.

4. The receiver of claim 1, wherein responsive to the control information the second control circuit retrieves a data payload from the input module, processes the data payload and transfers the processed data payload to a destination address identified by the control information.

5. The receiver of claim 1 wherein responsive to the match signal not being set, the second control circuit instructs the input module to discard the input data packet.

6. The receiver of claim 1 in which the digital data stream is an MPEG 2 encoded stream.

7. The receiver of claim 3 in which the input data packet comprises a packetized elementary stream.

8. The receiver of claim 4 in which the data payload comprises program specific information, and the receiver further comprises a filter controlled by the second control circuit for filtering sections in the data payload so as to retain only those data packets having sections required by the receiver.

9. The receiver of claim 1 in which first control circuit is a receiver processor, the second control circuit is a transport processor, and the third control circuit is a search engine.

10. A set top box including a receiver for demultiplexing a digital data stream, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, the receiver comprising:

an input module for receiving the digital data stream;

a memory for storing packet identifiers corresponding to data packets required by the receiver and separate from the input module;

a first control circuit for controlling the storage in the memory of the packet identifiers;

a second control circuit for extracting a packet identifier from a data packet in the digital data stream; and

a third control circuit for receiving the extracted packet identifier and determining whether such matches one of the packet identifiers stored in the memory, for setting a match

signal to the second control circuit responsive to a match, and for outputting an address in the memory responsive to a match, wherein the second control circuit accesses the address in the memory to retrieve control information associated with the packet identifier and controls processing of the input data packet responsive to the match signal by the input module.

11. A method of demultiplexing a digital data stream input to a receiver, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, comprising the steps of:

inputting the digital data stream;

storing in a memory separate from the data stream and under the control of a first control circuit, packet identifiers of data packets required by the receiver;

extracting, under the control of a second control circuit, a packet identifier from a data packet in the input digital data stream;

determining, under the control of a third control circuit, whether the extracted packet identifier matches one of the stored packet identifiers;

setting a match signal responsive to a match determined by the third control circuit;

outputting, responsive to a match and under the control of the third control circuit, an address in the memory;

accessing, under the control of the second control circuit, the address in memory;

retrieving control information associated with the packet identifier and stored at such address; and

demultiplexing, under the control of the second control circuit, the input data packet responsive to the match signal.

13. The method of claim 11 further comprising the step of:

transferring, under the control of the second control circuit, the input data packet to a destination address identified by the control information.

14. The method of claim 11 further comprising the steps of:

processing, under the control of the second control circuit, the input data packet in dependence on the control information; and

transferring, under the control of the second control circuit, the processed input data packet to a destination address identified by the control information.

15. The method of claim 11 in which the step of demultiplexing comprises discarding the input data packet responsive to the match signal not being set.

16. The method of claim 11 in which the digital data stream is an MPEG 2 encoded stream.

17. The method of claim 16 in which the input data packet comprises a packetized elementary stream.

18. The method of claim 16 in which the input data packet comprises program specific information, and wherein said demultiplexing step comprises:

filtering sections in the input data packet so as to retain only those data packets having sections required by the receiver.

19. The method of claim 11 in which the step of determining a match comprises systematically searching the memory.

20. A method of decoding a broadcast digital data signal in a set top box comprising:

inputting the digital data stream;

storing in a memory separate from the data stream and under the control of a first control circuit, packet identifiers of data packets required by the set-top-box;

extracting, under the control of a second control circuit, a packet identifier from a data packet in the input digital data stream;

determining, under the control of a third control circuit, whether the extracted packet identifier matches one of the stored packet identifiers;

setting a match signal responsive to a match determined by the third control circuit;

outputting, responsive to a match and under the control of the third control circuit, an address in the memory;

accessing, under the control of the second control circuit, the address in memory;

retrieving control information associated with the packet identifier and stored at such address; and

demultiplexing, under the control of the second control circuit, the input data packet responsive to the match signal.

21. A receiver for demultiplexing a digital data stream, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, the receiver comprising:

input circuitry for receiving the digital data stream;

a first data structure for storing addressing information that is accessed based on packet identifiers;

a second data structure for storing control information that is accessed based on addressing information extracted from the first data structure;

a first control circuit for extracting a packet identifier from a data packet in the digital data stream input to the input circuitry; and

a second control circuit for receiving the extracted packet identifier and determining whether such matches one of the packet identifiers in the first data structure, for setting a match signal to the first control circuit responsive to a match, and outputting addressing information responsive to a match, wherein the first control circuit accesses the second data structure to retrieve control information associated with the addressing information and demultiplexes the input data packet responsive to the match signal.

22. The receiver of claim 21 wherein responsive to the control information the first control circuit controls the transfer of the input data packet to a destination address identified by the control information.

23. The receiver of claim 21, wherein responsive to the control information the first control circuit processes the input data packet and transfers the processed input data packet to a destination address identified by the control information.

24. The receiver of claim 21 wherein responsive to the match signal not being set, the first control circuit discards the input data packet.

25. The receiver of claim 21 in which the digital data stream is an MPEG 2 encoded stream.

26. The receiver of claim 22 in which the input data packet comprises a packetized elementary stream.

27. The receiver of claim 23 in which the input data packet comprises program specific information, and the receiver further comprises a filter controlled by the first control circuit for filtering sections in the input data packet so as to retain only those data packets having sections required by the receiver.

28. The receiver of claim 21 in which first control circuit is a transport processor, and the second control circuit is a search engine.

29. A set top box including a receiver for demultiplexing a digital data stream, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, the receiver comprising:

input circuitry for receiving the digital data stream;

a first data structure for storing addressing information that is accessed based on packet identifiers;

a second data structure for storing control information that is accessed based on addressing information extracted from the first data structure;

a first control circuit for extracting a packet identifier from a data packet in the digital data stream input to the input circuitry; and

a second control circuit for receiving the extracted packet identifier and determining whether such matches one of the packet identifiers in the first data structure, for setting a match signal to the first control circuit responsive to a match, and outputting addressing information responsive to a match, wherein the first control circuit accesses the second data structure to retrieve control information associated with the addressing information and demultiplexes the input data packet responsive to the match signal.

30. A method of demultiplexing a digital data stream input to a receiver, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, comprising the steps of:

inputting the digital data stream;

storing control information in a first data structure;

storing packet identifiers and corresponding addressing information in a second data structure;

extracting, under the control of a first control circuit, a packet identifier from a data packet in the input digital data stream;

determining, under the control of a second control circuit, whether the extracted packet identifier matches one of the packet identifiers in the second data structure;

setting a match signal responsive to a match determined by the second control circuit;

outputting addressing information from the second data structure responsive to a match;

retrieving, under control of the first control circuit and based on the outputted addressing information, control information from the first data structure; and

demultiplexing, under the control of the first control circuit, the input data packet responsive to the match signal.

31. The method of claim 30 further comprising the step of:

transferring, under the control of the first control circuit, the input data packet to a destination address identified by the retrieved control information.

32. The method of claim 30 further comprising the steps of:

processing, under the control of the first control circuit, the input data packet based on the control information; and

transferring, under the control of the first control circuit, the processed input data packet to a destination address identified by the retrieved control information.

33. The method of claim 30 in which the step of demultiplexing comprises discarding the input data packet responsive to the match signal not being set.

34. The method of claim 30 in which the digital data stream is an MPEG 2 encoded stream.

35. The method of claim 34 in which the input data packet comprises a packetized elementary stream.

36. The method of claim 34 in which the input data packet comprises program specific information, and wherein said demultiplexing step comprises:

filtering sections in the input data packet so as to retain only those data packets having sections required by the receiver.

37. The method of claim 30 in which the step of determining a match comprises systematically searching the second data structure.

38. A method of decoding a broadcast digital data signal in a set top box comprising:

inputting the digital data stream;

storing, in a first data structure, control information;

storing, in a second data structure, packet identifiers required by the set-top-box and addressing information corresponding to the packet identifiers;

extracting, under the control of a first control circuit, a packet identifier from a data packet in the input digital data stream;

determining, under the control of a second control circuit, whether the extracted packet identifier matches one of the packet identifiers stored in the second data structure;

setting a match signal responsive to a match determined by the second control circuit;

outputting, responsive to a match, addressing information stored in the second data structure;

retrieving, under control of the first control circuit and based on the outputted addressing information, control information from the first data structure; and

demultiplexing, under the control of the first control circuit, the input data packet responsive to the match signal.

39. A receiver for processing a packetized digital data stream, the receiver comprising:

an input module to receive and process a data packet;

a memory;

a receiver processor to control storage of desired packet identifiers and associated control information in the memory; and

a transport controller having a transport processor to extract a packet identifier from a packet in the input module and a search engine to search the memory for a match of the extracted packet identifier to a desired packet identifier stored in the memory, wherein responsive to a match the transport processor retrieves from the memory control information

associated with the desired packet identifier stored in the memory and controls processing of the received data packet by the input module based on the retrieved control information.

40. The receiver of claim 39 wherein the transport processor generates a control signal to control processing of a packet by the input module based on associated control information retrieved from the memory.

41. The receiver of claim 40 wherein the input module discards a packet in response to the control signal.

42. The receiver of claim 40 wherein the input module descrambles a packet in response to the control signal.

43. The receiver of claim 40 wherein the input module passes a data payload to the transport controller in response to the control signal.

44. The receiver of claim 43 wherein the transport controller reformats the data payload based on the control information and passes the reformatted data payload to the input module for output in an alternative output stream.

45. A receiver for processing a packetized digital data stream, the receiver comprising:

means for receiving a data packet in the digital data stream;

means for retrieving control information associated with a received data packet; and

means for controlling processing of a received data packet by the means for receiving a data packet.

46. The receiver of claim 45 wherein the means for retrieving control information comprises a memory storing packet identifiers and control information associated with desired data packets in the digital data stream, a search engine and a transport processor.

APPENDIX B
Final Office Action

TLB

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/239,907	01/29/1999	ANDREW MACCORMACK	858063.435	6683

500 7590 02/08/2006

EXAMINER
BELIVEAU, SCOTT E

ART UNIT	PAPER NUMBER
2614	

DATE MAILED: 02/08/2006

SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVE
SUITE 6300
SEATTLE, WA 98104-7092

Please find below and/or attached an Office communication concerning this application or proceeding.

2 - month Response Due: Apr. 6, 2006
3 - month Response Due: May 6, 2006
Notice of Appeal Due: Aug. 6, 2006
(6 - month period ends) Will Go Aban
(3 - month extension of the time required)

FINAL REJECTION

ENTERED IN DOCKET RR

Office Action Summary	Application No.	Applicant(s)	
	09/239,907	MACCORMACK ET AL.	
	Examiner	Art Unit	
	Scott Beliveau	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-11 and 13-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11,13-42,45 and 46* is/are rejected.

7)☒ Claim(s) *43 and 44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "first control circuit" or receiver processor (IA: Page 15, Para. 5) (ex. claims 1, 10, 11, etc.), as well as the particular "methods" being performed by these the illustrated system components (ex. claims 11, 13-15, 18, 19-20, 30-33, and 36-37) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 3-10 and 39-42, 45, and 46 have been considered but are moot in view of the new ground(s) of rejection.

3. Applicant's arguments filed 09 May 2005 have been fully considered but they are not persuasive with respect to the rejection of claims 11 and 13-20 under Dokic in view of the ADSP-2100 Family User's Manual – Chapter 4: Data Transfer.

With respect to applicants' arguments regarding claims 11 and 13-20, applicant's argue that the interpretation of the claimed memory as including memory "205" and data buffers "200" and "202" is unreasonable because they do not store "packet identifiers corresponding to data packets required by the receiver". Applicants note that the buffers load all packets in the transport stream, whether the packets are required or not. However, as argued, if all of the packets are stored in the aforementioned buffers, then it would logically follow that both those which are required as well as those which are not required would be stored (even if only temporarily); thereby meeting the claimed limitations. With respect to the buffers "200" and "202" not being separate from the data stream, the examiner relies upon a broad interpretation of what is meant by separate from in order for such a limitation to be supported by the specification as originally filled. The instant application similarly buffers and/or stores received packets in memory as well as stores packet identifiers corresponding to data packets required by the receiver in memory "400". Taking a very narrow interpretation of what is meant by "separate from" (ex. the very fact that the particular information is buffered and/or stored results in it not being "separate from") would render the claims as being not

enabled by the specification as originally filled. Rather, the examiner is interpreting "separate from" simply to mean that both the data stream and the memory are distinctive entities in their own rights. For example, the memory is a distinctive or separate element regardless of its particular storage of data.

4. Applicant's arguments filed 09 May 2005 have been fully considered but they are not persuasive with respect to the rejection of claims 21-38 under Dokic in view of Blatter et al.

With respect to applicant's arguments regarding the combined teachings of Dokic and Blatter, the examiner respectfully disagrees. With respect to "outputting address information", examiner respectfully refers applicants to the Blatter reference for this teaching. In particular, the examiner refers applicant to the section of Blatter which discloses that the particular usage of memory mapping between control and/or encryption information and particular packet identifies which are retrieved in association with the processing of the received packets (Blatter: Col 4, Line 56 – Col 5, Line 18). Accordingly, it is the examiner's understanding that the particular memory address information would need to be "outputted" in conjunction with the processing of the received packets.

In response to applicant's argument regarding the particular physical combination of elements between Dokic and Blatter such that the particular combination would render the Dokic system unsuitable for its intended purpose, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871

(CCPA 1981). In the instant case, the DSP of Dokic comprises a "first memory structure" [205] that stores information that enable the DSP to demultiplex and appropriately process the received transport stream by identifying packets of interest. The Blatter reference discloses a similar structure [45] which is construed as meeting both the claimed "first data structure" and "second data structure" in so far as it comprises both "addressing information that is accessed based on packet identifiers" and "control information that is accessed based on addressing information extracted from the first data structure" (Blatter: Col 4, Line 56 – Col 5, Line 18) in conjunction with the particular usage of memory mapping between control and/or encryption information and particular packet identifies which are retrieved in association with the processing of the received packets. The Dokic reference discloses an MPEG signal demultiplexing system using a decoupled architecture such that the DSP demultiplexes the received stream and provides a limited interpretation of the information received for subsequent display. The decoupled architecture "speeds up" the processing over a non-decoupled architecture. However, the reference, does not particularly teach away from all modifications to what may be considered as a necessary part of a limited interpretation process in order to generate a usable picture or other modifications associated with faster processing of PSI information. For example, if an encrypted stream such as that associated with the contemplated video-on-demand service is received, it would be necessary to descramble that image prior to display. Accordingly, the particular modification to the existing memory structure of Dokic so as to further comprise additional structural information associated with the particular interpretation of a received transport stream is not considered to be taught away from by the reference itself.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the Dokic reference is directed towards MPEG signal demultiplexing using a decoupled architecture. The Dokic reference further utilizes PSI information. The analogous art Blatter reference teaches a system and method which further advantageously speeds the processing of PSI information and further advantageously facilitates the processing of both encrypted and/non-encrypted information.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1 and 3-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As set forth in the specification as well as applicant's previous arguments, the "third control circuit" corresponds to the illustrated search engine [322] and the input module corresponds to the illustrated input module [100]. The specification sets forth that the search engine generates a match signal responsive to finding a match and subsequently instructs the "second control circuit" or transport processor [320] to access a particular address for information needed so as to control the input module [100] to process the received signal which may include the particular descrambling of the received information (IA: Page 9, Para 7 – Page 12, Para. 2; Page, 20, Para. 3 – Page 21, Para. 2). The claim sets forth that the "second control circuit" or transport processor [320] further "controls processing of the input data packet responsive to the match signal by the input module". However, as disclosed in the prior section of the specification, while the "second control circuit" is operable to control processing of the input data packet by the input module responsive to the match signal, the match signal is not generated by the input module. Rather, the particular match signal as disclosed in the specification and required by the claim to be generated by the "third control circuit" (ex. a "third control circuit . . . for setting a match signal to the to the second control circuit responsive to a match"). No further art rejection is being applied in light of the logical inconsistency required by the claim; given that the claim initially sets forth that the "third control circuit" is responsible for generating the match signal and latter claims that the distinctive input module is responsible for the match signal.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 39-41, 45, and 46 are rejected under 35 U.S.C. 102(e) as being anticipated by Dokic (US Pat No. 5,959,659).

Claim 39 is rejected wherein the Dokic reference discloses a "receiver" [100] for "processing a packetized digital data stream".. As illustrated in Figures 3 and 5, the "receiver" [100] comprises an "input module" [104] to "receive and process a data packet" associated with an MPEG-2 transport stream" a "memory" [205], and a "receiver processor" [106] to "control storage of desired packet identifiers and associated control information in the memory" (Col 8, Lines 24-31; Col 13, Lines 13-26). The receiver further comprises a "transport controller" [102] having a "transport processor" [204] to "extract a packet identifier from a packet in the input module" and a "search engine to search the memory for a match of the extracted packet identifier to a desired packet identifier stored in the memory". Subsequently, "responsive to a match the transport processor retrieves from the memory control information associated with the desired packet identifier stored in memory" such as control information serving to designate the particular packet type and "controls processing of the received data packet by the input module based on the retrieved control information" such that it is directed to the appropriate packet buffer [206/208/210] (Col 7, Line 49 – Col 9, Line 6).

Claim 40 is rejected wherein the "transport processor generates a control signal to control processing of a packet by the input module based on associated control information retrieved from the memory" (Col 8, Lines 53-67).

Claim 41 is rejected wherein the "input module discards a packet in response to the control signal" (Col 8, Lines 64-67).

In consideration of claim 45, Figure 3 of the Dokic reference discloses a "receiver" [1000] for "processing a packetized digital data stream". The "means for receiving a data packet" [112/114], a "means for retrieving control information associated with a received data packet" [102], and a "means for controlling processing of a received data packet by the means for receiving a data packet" [106].

Claim 46 is rejected wherein the "means for receiving control information" [102] (Figure 5) comprises a "memory for storing packet identifiers and control information associated with desired packets in the digital data stream" [205] (ex. information identifying the particular PID as well as information identifying the particular type of PID), a "search engine" and a "transport processor" [204] (Col 8, Lines 7-67).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 11 and 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dokic (US Pat No. 5,959,659) in view of the ADSP-2100 Family User's Manual – Chapter 4: Data Transfer.

In consideration of claims 11 and 20, the Dokic reference discloses a method of "demultiplexing" or "decoding a digital data stream" wherein the "digital data streams . . . including data packets having a packet identifier" such as those defined by the MPEG-2 specification (Col 1, Lines 19-23; Col 2, Lines 45-65). The method comprises "inputting the digital data stream" (Figure 3; Col 5, Line 60 – Col 6, Line 9) and "storing in a memory separate from the data stream" [205] (Figure 3) and "under control of a first control circuit" [106], the "packet identifiers that correspond to data packets required by the receiver" (Col 8, Lines 28-31 and 58-60; Col 9, Lines 10-23). The system "extracts under the control of a second control circuit" [204], a "packet identifier from a data packet in the input digital stream", "determines, under the control of a third control circuit" [204] "whether the extracted packet identifier matches one of the stored packet identifiers", sets a match signal responsive to a match determined by the third control circuit", and "demultiplexes under the

control of the second control circuit, the input data packet responsive to the match signal" (Col 8, Lines 20-52; Col 9, Lines 18-43).

With respect to the limitation pertaining to "outputting an address", the Dokic reference does not explicitly disclose nor preclude details pertaining to the retrieval of information through a "memory address". The reference explicitly discloses that the preferred embodiment of the digital signal processor is a DSP2111 manufactured by Analog Devices® (Col 7, Lines 53-55). The ADSP-2100 Family User's Manual – Chapter 4 describes that the circular buffers rely on "addresses" in order to determine where to locate the next piece of information in a circular buffer may be located (Sections 4.2.3 – 4.3.2). Accordingly, it would have obvious to one of ordinary skill at the time of the invention to utilize the teachings of the ADSP-2100 User's Manual such that the embodiment would implicitly "output an address in the memory responsive to a match" in order to know where in the on-board memory [200/202/205] to retrieve the "entire packet" comprising both the identifier and "control information associated with the packet identifier" for the purposes of implementing the preferred embodiment using components explicitly disclosed by Dokic.

As to the limitation pertaining to the "control information", the claimed language is not limiting other than to require that the "control information" is something that is "associated with the packet identifier". The Dokic reference teaches that the MPEG-2 transport stream may comprise packets of "control information" such as the program map table (PMT) or program association table (PAT) from the MPEG-2 transport stream (Col 4, Lines 22-27). These program specific information (PSI) tables are associated with reserved packet identifiers (PID) (ISO/IEC 13818-1: Section 2.4.4). As such, the Dokic reference teaches

that the PID from the received packet is parsed from the transport packet to identify the type of data carried by the transport packet. Accordingly, "control information" may be temporarily stored in the packet buffers [200/202] prior to being transferred to the host processor [106] (Col 9, Lines 29-43).

Alternatively, it is further noted that the packet header may further comprise "control information" in the form of timing information (PCR) used in the decoding of the payload. The packet buffers [200/202] or "memory" are disclosed to store the entire transport packet comprising "control information associated with the packet identifier" (Col 7, Lines 66-67 – Col 8, Lines 1-4). The Dokic reference goes on to suggest that either the "entire packet" or the payload may be forwarded from the "memory" (Col 9, Lines 39-43). The claim language is subsequently not limiting such that the "entire packet" comprising both the identifier and the "control information associated with the identifier" contained within the packet header may be "accessed" and "demultiplexed".

Claims 13 and 14 are rejected in view of Figure 5 wherein "the second control circuit" [204] controls the transfer of and/or processes "the input data packet to a destination" such as data buffers [206/208/210] or host microprocessor as "identified by the control information" (Col 8, Lines 31-37, 53-67). It is taught that should the "input data packets" contain private data, the entire packet will either be "transferred". Alternatively, the packet may be "processed" such that only the payload data is "transferred" (Col 9, Lines 39-53).

Claim 15 is rejected wherein the Dokic reference teaches that the packet is "discarded" if a "match" is not found (Col 8, Lines 51-52)

Claims 16 and 17 is rejected wherein the reference teaches a method/apparatus for the interpretation and demultiplexing of received MPEG-2 transport packets (Col 7, Lines 49-59). The MPEG-2 standard (incorporated by reference) defines a transport stream as being logically constructed from a "packetized elementary stream" or PES packets.

In consideration of claim 18, the component elements of the "input" data stream are well known in the art, as evidenced by the MPEG-2 specification,. Figures 1-2 of the Dokic reference illustrates that the "input data packet comprises program specific information" or PSI tables (Col 2, Lines 3-19). As aforementioned, the receiver uses these PSI tables to derive PIDs that corresponds to desired programming which are subsequently used by the "second control circuit" [204] to "retain only those data packets having sections required by the receiver" (Col 2, Lines 29-44; Col 8, Lines 20-31, 48-52).

Claim 19 is rejected wherein the "third control circuit" [204] "systematically" searches the transport packet buffers [200/202] for a "match". Figures 6A-C further illustrate a "systematic" method for "searching the memory" in conjunction with the demultiplexing process.

12. Claims 21-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dokic (US Pat No. 5,959,659) in view of Blatter et al. (US Pat No. 5,844,595).

In consideration of claims 21 and 29, as aforementioned, the Dokic reference discloses a decoder that may function as a "set top box" or "receiver for the demultiplexing digital data streams . . . including data packets having a packet identifier" such as those defined by the MPEG-2 specification (Col 1, Lines 19-23; Col 2, Lines 45-65). Figure 3 illustrates a block diagram of the "receiver" architecture comprising: "input circuitry for receiving the digital

data stream" [112] (Col 6, Lines 10-12), a demultiplexing section [104], and a control section [108] (Col 5, Line 60 – Col 6, Line 9). The demultiplexing section, as illustrated in Figure 5 comprises a data structure [205] for storing packet identifiers that correspond to data packets required by the receiver (Col 8, Lines 26-31) and a "first" and "second control circuits" [204] of the digital signal processor [102] for "extracting a packet identifier from a data packet in the digital data stream input", "determining whether such matches one of the packet identifiers in the first data structure", and "responsive to a match" is operable to "demultiplex the input data packet" (Col 8, Lines 20-52; Col 9, Lines 18-43).

The reference, however, does not explicitly disclose nor preclude the particulars pertaining to the "first" and "second data structure" as particularly claimed nor does it disclose the particular usage of encryption/decryption in conjunction with the MPEG-2 transport as is understood in the art. The Blatter et al. reference discloses the usage of encryption/decryption in conjunction with a MPEG demultiplexor comprising a "first" [45] and "second data structure" [45] wherein the "control information" or decryption information associated with the "second data structure" [45] is memory mapped or "accessed based on addressing information extracted from the first data structure" (Col 4, Line 56 – Col 5, Line 19). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the data structure [205] of Dokic reference to comprise a "first" and "second data structure" such as those employed by Blatter et al. such that "responsive to a match" the "addressing information" associated with the "control information" is "outputted" and "retrieved" for the purpose of advantageously providing a means to employ encryption/decryption in conjunction with transmitted MPEG video and to

further provide a low-overhead mechanism by which processes can synchronize and communicate while reducing I/O data movement.

Claims 30 and 38 are rejected in view of the rejection of claims 21 and 29. The "method of demultiplexing a digital data stream" in conjunction with a "set-top-box" is met wherein the reference teaches the following steps: "inputting the digital data stream" (Dokic: Figure 3; Col 5, Line 60 – Col 6, Line 9), "storing . . . packet identifiers required by the receiver in a second data structure" [205] (Col 8, Lines 28-31 and 58-60; Col 9, Lines 10-23), and "determining", "extracting", and "demultiplexing" under the control of a "second" and "third control circuit" packets responsive to a "match" (Dokic: Col 8, Lines 20-52; Col 9, Lines 18-43). As aforementioned, the Dokic reference does not explicitly disclose the particular usage of "outputting addressing information" in conjunction with a "first" and "second data structure". The Blatter et al. reference discloses the usage of a "first" [45] and a "second" data structure" [45] whereupon addressing information from the "second data structure" [45] may be utilized to access "control information" associated with the decryption of packets from the "first data structure" [45]. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Dokic reference to further employ a "first" and "second data structure" that employs memory mapping techniques such as those employed by Blatter et al. for the purpose of advantageously providing a means to employ encryption/decryption in conjunction with transmitted MPEG video and to further provide a low-overhead mechanism by which processes can synchronize and communicate while reducing I/O data movement.

In consideration of claims 22-23 and 31-32, the Blatter et al. reference further discloses that the "control information" further identifies "destination address information" (Col 5, Lines 5-8). Accordingly, "the second control circuit" [204] controls the transfer of and/or processes "the input data packet to a destination" such as data buffers [206/208/210] or host microprocessor as "identified by the control information" (Dokic: Col 8, Lines 31-37, 53-67).

Claims 24 and 33 are rejected wherein the Dokic reference teaches that the packet is "discarded" if a "match" is not found (Col 8, Lines 51-52)

Claims 25-26 and 34-35 are rejected wherein the reference teaches a method/apparatus for the interpretation and demultiplexing of received MPEG-2 transport packets (Col 7, Lines 49-59). The MPEG-2 standard (incorporated by reference) defines a transport stream as being logically constructed from a "packetized elementary stream" or PES packets. The instant application further supports this definition (Page 2, Lines 5-8).

In consideration of claims 27 and 36, the component elements of the "input" data stream are well known in the art, as evidenced by the MPEG-2 specification,. Figures 1-2 of the Dokic reference illustrates that the "input data packet comprises program specific information" or PSI tables (Col 2, Lines 3-19). As aforementioned, the receiver uses these PSI tables to derive PIDs that corresponds to desired programming which are subsequently used by the "second control circuit" [204] to "retain only those data packets having sections required by the receiver" (Dokic: Col 2, Lines 29-44; Col 8, Lines 20-31 and 48-52).

Claims 28 and 37 are rejected wherein the "first" and "second control circuits" [204] are embedded within a digital signal processor [106] that is coupled to a PAL [118].

Accordingly, the digital signal processor [106] functions as both a "search engine" to identify buffered packets and a "transport processor" to move the packets into the appropriate buffer as aforementioned (Dokic: Col 8, Lines 20-52).

13. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dokic (US Pat No. 5,959,659) in view of Bestler et al. (US Pat No. 5,602,920).

In consideration of claim 42, the Dokic reference does not particularly disclose that the "input module" [104] further "descrambles a packet in response to the control signal". The Bestler et al. reference discloses a combined DCAM and transport demultiplexer [20] or "input module" wherein the "input module descrambles a packet in response to the control signal" (Bestler et al.: Col 3, Lines 7-44; Col 4, Lines 25-59; Col 4, Line 66 – Col 5, Line 17). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made so as to modify the "input module" [104] so as to further comprise a descrambler which "descrambles a packet in response to the control signal" for the purpose of providing/enabling greater flexibility in the types of programming (ex. premium, PPV, or other forms of scrambled programming) with which the Dokic system can process and to particularly do so using a single circuit optimized to perform both demultiplexing and conditional access functions (Bestler et al.: Col 1, Lines 49-67).

Allowable Subject Matter

14. Claims 43 and 44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In particular, based upon the interpretation of the

"input module" and the "control signal" as relied upon in the rejection of claims 39 and 40, the "input module" of Dokic does not "pass a data payload to the transport controller in response to the control signal".

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made.

- The Robbins et al. (US Pub No. 2004/0004977 A1) reference discloses a circuit and method for demultiplexing in a receiver a digital data stream including at least two different types of data.
- The MacCormack (US Pat No. 6,859,850) reference discloses a controller for controlling direct memory access.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to

37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Beliveau whose telephone number is 571-272-7343. The examiner can normally be reached on Monday-Friday from 8:30 a.m. - 6:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John W. Miller can be reached on 571-272-7353. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Scott Beliveau
Examiner
Art Unit 2614

SEB
February 6, 2006

Notice of References Cited	Application/Control No. 09/239,907	Applicant(s)/Patent Under Reexamination MACCORMACK ET AL.	
	Examiner Scott Beliveau	Art Unit 2614	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2004/0004977	01-2004	Robbins et al.	370/535
*	B	US-6,859,850	02-2005	MacCormack, Andrew	710/52
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

APPENDIX C

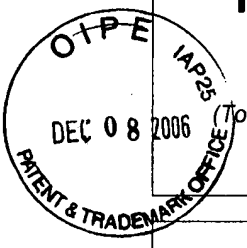
Related Proceedings Appendix

There are no known related proceedings.

12-1-06

EXPRESS MAIL NO. EV889129405US

ZFW AF



TRANSMITTAL FORM

(To be used for all correspondence after initial filing)

Application Number	09/239,907
Filing Date	January 29, 1999
First Named Inventor	Andrew MacCormack
Art Unit	2623
Examiner Name	Scott E. Beliveau
Attorney Docket No.	858063.435

ENCLOSURES (*check all that apply*)

- [X] Fee Transmittal Form
  - [X] Fee Attached
- [ ] Amendment/Response
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [X] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement and Transmittal
- [ ] Cited References
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Response to Missing Parts/Incomplete Application
- [ ] Drawing(s)
- [ ] Request for Corrected Filing Receipt
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation, Change of Correspondence Address
- [ ] Declaration
- [ ] Statement under 37 CFR 3.73(b)
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [X] Appeal Communication to TC *(Appeal Notice, Brief, Reply Brief)*
- [ ] Proprietary Information
- [ ] Status Letter
- [X] Return Receipt Postcard
- [ ] Other Enclosure(s) *(please identify below)*:

_____

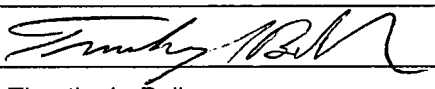
_____

_____

_____

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Seed Intellectual Property Law Group PLLC	Customer Number	00500
Signature			
Printed Name	Timothy L. Boller		
Date	December 8, 2006	Reg. No.	47,435

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Signature		
Typed or printed name		Date:

SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

876468_1.DOC

EXPRESS MAIL NO. EV889129405US

Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2006

OIPE 12AP25 DEC 08 2006 PATENT & TRADEMARK OFFICE

Complete if Known	
Application Number	09/239,907
Filing Date	January 29, 1999
First Named Inventor	Andrew MacCormack
Examiner Name	Scott E. Beliveau
Art Unit	2623
Attorney Docket No.	858063.435

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) **2090**

METHOD OF PAYMENT (check all that apply)

☒ **Check** ☐ Credit Card ☐ Money Order ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 19-1090 Deposit Account Name: Seed IP Law Group PLLC

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☐ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☒ Charge any underpayments or credit any overpayments

Warning: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION (All the fees below are due upon filing or may be subject to a surcharge.)

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	_____
Design	200	100	100	50	130	65	_____
Provisional	200	100	0	0	0	0	_____

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims		Extra Claims		Fee ($)		Fee Paid ($)
_____	-20 or HP =	_____	X	_____	=	_____

HP = highest number of total claims paid for, if greater than 20.

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
_____	_____

Indep. Claims		Extra Claims		Fee ($)		Fee Paid ($)
_____	-3 or HP =	_____	X	_____	=	_____

HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

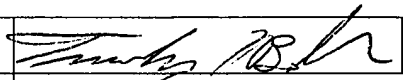
If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)) the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		Extra Sheets		Number of each additional 50 or fraction thereof		Fee ($)	Fee Paid ($)
_____	-100 =	_____	/50 =	_____ (round **up** to a whole number)	x	_____	_____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	_____
Other (e.g., late filing surcharge): Appeal Brief Fee	500
Petition for Extension of Time (4 mos.)	1590
_____	_____

SUBMITTED BY

Signature		Registration No. (Attorney/Agent)	47,435	Telephone	206-622-4900
Name (Print/Type)	**Timothy L. Boller**			Date	December 8, 2006

876531_1.DOC